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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,262	07/15/2003	Nicolas Demange	854063.523C1	9726

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EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,262	DEMANGE ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/365,178.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restriction

Applicant's election without traverse of claim 16-36 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-36 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors, such as in claim 17, line 5, "said transistors" should be "said transistor", "first and second conductive region" should be "first and second conductive regions", "first and second plate" should be "first and second plates". "said capacitors" should be "said capacitor", "said control electrodes" should be "said control electrode", etc. Similar error also found in the remaining claims, such as "first and second plate" should be "first and second plates", etc. Appropriate action is required to correct all the antecedent and grammatical errors including errors that are not listed by the examiner.

Claims 24-36 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In view of the specification, the meaning of "first and second capacitors being

positioned in a firs plane that is ***transverse*** to a second plane in which the second and third capacitors are position" is not clear.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 17-36 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,300,654. Although the conflicting claims are not identical, they are not patentably distinct from each other because merely rearranging the sentence, such as "a plurality of bit lines connected to said second conductive region" to "said second conductive of each of said MOS transistors being connected a respective bit line" etc does not changed the scope of claimed invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Brassington et al. 5,350,705, cited by applicant.

Bassington discloses a memory array, comprising:

a plurality of stacked cells 12. 22 (40/44/46/16, 42/44/46/16, col. 5, lines 28+ and figs. 2+) each cell including:

a MOS transistor 14, 24 formed in an active region of a substrate of semiconductor material 36,

a capacitor 12, 22 formed above the active region, each of MOS transistor 14, 24 having a first and a second conductive regions 32, 38, 34 and a control electrode 20, 26 and each of capacitor having a first and a second plates 40/46, 42/46 separated by a dielectric material region 44, the first conductive region 32/34 each of MOS transistor being connected to first plate 40, 42 of a respective capacitor 12, 22,

a plurality of bit lines 18 connected to said second conductive regions 38 of MOS transistors 14, 24 of respective cells 12, 22 of the plurality of stacked cells 12, 22,

a plurality of word lines 20, 26 connected to control electrodes 20, 26 of respective MOS transistors 14, 24 of the plurality of stacked cells 12, 22, col. 6, lines 5+,

a plurality of plate (drive) lines 16/46 connected to second plate 46 of respective capacitor, the plate lines 16 running perpendicular to bit lines 18 and parallel to word lines 26, wherein a pair of cells 12, 22 adjacent to each other in a direction parallel to bit lines 18 share a same dielectric material region 44 and a same third conductive region, forming second plates of capacitors of said pair of cells, see figs. 1-3.

Claims 24-26, 28-32 and 34-36 are rejected under 35 U.S.C. § 102(b) as being anticipated by Okudaira et al. 5,418,388, cited by applicant.

Okudaira et al. discloses a memory array, comprising:

a substrate of semiconductor material 1, fig. 1+ and col. 8, lines 55-68 and col. 9, lines 1+,

a first stacked cell comprising a first transistor 3 formed in a first active region 6b of the substrate 1 and a first capacitor 14/15/16 formed above the first active region, the first capacitor having a first and a second plates separated 14/16 by a first dielectric region 15 (a ferroelectric material), col. 9, lines 29-35,

a second stacked cell comprising a second transistor formed in a second active region 6c of the substrate 1 and a second capacitor 14/15/16 formed above the second active region 6c, the second capacitor having a first and a second plates 14/16 separated by a second dielectric region 15 that is continuous with the first dielectric region 15, the second plate 16 of the second capacitor being continuous with the second plate 16 of the first, capacitor, and

a third stacked cell comprising a third transistor formed in a third active region 6d of the substrate and a third capacitor formed above the third active region 6d, the third capacitor having a first and a. second plates 14, 16 separated from each other by a third dielectric 15 region that is continuous with the first and second dielectric regions 15, the second plate 16 of the third capacitor being continuous with the second plates 16of the first capacitor and the second capacitor, the first and second capacitors being positioned in a first plane that is transverse to a second plane in which the second and third capacitors are positioned, see fig. 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27 and 33 are rejected under 35 U.S.C 103 as being unpatentable over Okudaira et al. as applied to claims 24-26, 28-32 and 34-36 above, and further in view of Brassington et al. 5,350,705, cited by applicant.

The difference between the references applied above and the instant claim(s) is:Okudaira teaches a ferroelectric capacitor DRAM device having continuous capacitor dielectric layer between first and second plates for each capacitor and word line is perpendicular to bit line (fig. 72) but does not teaches that dielectric band extending in a first direction and second plates are part of a plate line extending in the first direction in parallel to the dielectric band. However, Brassington et al. teaches at fig. 2 that a plate (drive) line 16/46 extending in the first direction in parallel to the dielectric band 44.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references teachings with a plate (drive) line extending in the first direction in parallel to the dielectric band as taught by Brassington et al. because plate line must formed on the capacitor dielectric layer to form a capacitor and cover as much as capacitor dielectric layer to obtain a larger capacitor, hence, plate line obviously must extending in the same direction of the dielectric band.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is (703) 306-3329 and Fax number (703) 872-9306. Group receptionist telephone number 703-308-0956.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for this Group is (703) 872-9306.

hjt

3/2/04

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800